Study of Cross-Coupled Current Conveyor Based CMOS Transimpedance Amplifier for Broadband Data Transmission

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Abstract- A novel cross-coupled current conveyor based CMOS transimpedance amplifier (TIA) design to obtain an input capacitance load insensitive and very low noise structure is presented. This paper presents a new topology to offset the large junction capacitance brought by photodiode and enhance the bandwidth. It is achieved by creating a “zero differential impedance” at the input node of a TIA. This input stage is based on a cross-coupled current conveyor structure. The TIA relaxes the bandwidth limitation at the input node, and exhibits a stable performance over a wide range capacitive load. This cross-coupled structure also brings a huge improvement in noise performance.

Keywords - Transimpedance amplifier, Cross-coupled current conveyor, Bandwidth, Noise performance, Zero differential impedance.

I. INTRODUCTION

Large capacity optical transmission system require high speed optical receiver. They contain a photodetector and a Transimpedance (TZ) amplifier, which is used to convert the optical signal into electrical signals in the front end of optical fiber communication. Therefore, a high-speed TZ amplifier is a very important part for designing optical receiver. Many early research groups have been successful in designing and fabricating a low-cost and high integrated circuit by on-chip silicon technology [1]-[4]. Silicon technology has many advantages on more expansive technologies such as SiGe bipolar and BiCMOS or the GaAs technology [5]. In high speed opto-electronic receivers has most suitable preamplifier that is Transimpedance amplifier. To achieve high bandwidth, gain and impedance transformation use TIA [6]. All available technology such as GaAs [7], [8] or SiGe bipolar technology [9] are not suitable for low cost, high volume production because of high power consumption and relatively large chip area. But CMOS process technology gives low power, low cost and high yield. TIA has many designing parameters such as bandwidth, high transimpedance gain, low noise, low power consumption and small group delay variation [10].
Current to Voltage Signal Conversion

Reshapes Signal for Input to Digital System

Photodiode

Transimpedance Amplifier (TIA)

Limiting Amplifier (LA)

Output buffer (OB)

Automatic Gain Control (AGC)

To Maintain Signal Linearity and Gain Level

Output Derive and Circuit

Optical In

Electrical Out

Fig.1. Optical Receiver

The optical signal from the fiber is received by photodiode, which produces a small output current proportional to the optical signal as shown in Fig.1. Current is amplified and converted to a voltage using Transimpedance Amplifier. The voltage signal is further amplified by Limiting Amplifier (LA) or Automatic Gain Control Amplifier (AGC). The LA and AGC Amplifier are collectively known as Main Amplifier (MA) or Post Amplifier.

Fig.2. Basic Transimpedance Amplifier Structure

Optical photodiode or optical photoconductive detectors are current sources, with the current produces being proportional to the light intensity illuminating them. This amplifier is used for translating the output from a very high impedance current source to a low impedance op amp output so that it is called Transimpedance Amplifier that is usually operated at very high gain. The Fig.2. shows the basic transimpedance amplifier structure. The drawback of operating any op amp with very high gain is that its frequency response is greatly reduced because an op amps gain and bandwidth are inversely proportional to each other. Therefore large bandwidth is critical to achieve for optical transmission [11]-[14]. The preceding photodiode is introducing very large capacitance at input node that restrict the bandwidth. Large area photodiode is used to capture sufficient optical power and area is directly proportional to capacitance, that’s why researcher introduce various TIA architecture that explore different input stages for isolating the large input capacitance of the photodiode. There are many architecture such as common gate (CG) input gate [15], regular cascade (RGC) stage [13], or CG feed forward topology containing feedback. For bandwidth enhancement we also use inductive peaking [16]-[19] and capacitive degeneration [13].

II. LITERATURE REVIEW
Chang, Z [1989] discussed a low noise wideband transimpedance amplifier which matches an inductive source that’s makes it difficult to design such as an amplifier to meet both low-noise and stability requirements that’s why he proposed a novel feedback configuration. The use of this configuration gives good noise performance and stability. The amplifier is suitable to be implemented in bipolar junction transistor technology and can be used as the preamplifier in an up conversion radio receiver. A transimpedance of 220 KΩ and total equivalent input noise current density between 0.35 to 0.75 pA/√Hz have been achieved. [17].

Feng Tso Chien et al [1999] introduced a capacitive peaking (C-Peaking) technique to increase the bandwidth and give its analytical model that determine the peaking capacitance in the Butterworth type transimpedance amplifier design. Simulation results shows that 3-dB bandwidth of the transimpedance amplifier is enhanced from 1.1 to 2.3 GHz without reducing its low-frequency gain and also shows a measured linear gain of 0.95k with a wide dynamic injected current [18]. Hasan Rezaul M. S. et al [2005] discuss a design of a novel inductively peaked broad band transimpedance amplifier architecture that has high noise immunity, wide dynamic range and low power dissipation and bandwidth that is also extended using the inductive peaking technique. By this technique author shows the result -3dB bandwidth of 3.5 GHz with a transimpedance gain of 60dB ohms, suitable for application in optical receivers. Output peak to peak voltage swing of around 400mV for input current swing of 100 A gives a dynamic range of the amplifier and the output noise voltage spectral density was 12nV/√Hz while the input referred noise current spectral density was below 20 pA/√Hz within the amplifier frequency band which shows that this amplifier has high noise immunity [16].

Wei-zen chen et al [2006] present a design of an optical receiver analog front end circuit capable of operating at 2.5 Gb/s a low cost digital CMOS process. He discussed that several gain-bandwidth enhancement techniques that boost overall performance specially high gain and wide bandwidth. Design a receiver using active inductors instead of using bulky inductors at 2.5 Gb/s, gives input sensitivity of the receiver front end is 16µA with bit – error- rate less than $10^{-12}$ and output swing is about 250 mV (single-ended). By using Active inductor chip area can be greatly reduced and the Transimpedance Amplifier and Post Limiting Amplifier is fabricated on single chip is possible [19].

El-sayed A. M. Hasaneen et al. [2007] discuss an accurate and efficient technique using on-chip spiral inductor to enhance the bandwidth of the Transimpedance amplifier also shows the effect of the varying of the inductor inductance on the bandwidth extension. By using on chip spiral inductors results shows that the bandwidth of the transimpedance amplifier is greatly improved additionally by 47% without on-chip inductor the bandwidth is 27.76 GHz and it is extended up to 47.009 GHz. To reduce the non idealistic on the on-chip inductor total load resistance is partitioned the inductor series resistance and an external load resistance that improve the bandwidth with no additional power dissipation [20]. Chih-Fan Liao et al [2008] introduced a 40 Gb/s transimpedance- AGC amplifier and CDR circuit and verified in 90 nm digital CMOS, demonstrating the potential of standard CMOS technology for receivers operating at tens of gigabits per second. This design methodology resolve a number of issues and provide promising performance with lower power dissipation compared to similar circuits realized in SiGe, InP, or GaAs technologies and analysed the RTRN, showing that the bandwidth is extended by a larger factor compared to using the shunt-series peaking technique, especially in cases when the parasitic capacitance is dominated by the next stage. Design is fabricated in 90 nm digital CMOS technology, the overall amplifier consumes 75 mW and the CDR circuit consumes 48 mW excluding the output buffers, all from a 1.2 V supply [21].

Jin-Sung Youn et al [2009] present a high-speed monolithically integrated optical receiver with 4.25-Gb/s optical data fabricated with 0.13-µm standard complementary metal–oxide–semiconductor (CMOS) technology. The optical receiver consists of a CMOS-compatible avalanche photodetector (CMOS-APD) and a transimpedance amplifier (TIA). That provides high responsivity as well as large bandwidth and Its bandwidth is further enhanced by the TIA having negative capacitance, which compensates undesired parasitic capacitance with optical power of 5.5 dBm [22]. Joohwa Kim [2010] et al discussed that A 40-Gb/s transimpedance amplifier (TIA) using multistage inductive-series peaking for low group-delay variation and a bandwidth- enhancement technique using inductive-series -networks is analyzed. This is a design method for low group delay constrained to 3-dB bandwidth enhancement is suggested. The TIA is implemented in a 0.13µ m CMOS process and achieves a 3-dB bandwidth of 29 GHz. The transimpedance gain is 50 dB Ω, and the transimpedance group-delay variation is less than 16ps over the 3-dB bandwidth.
The chip occupies an area of 0.4 mm², including the pads, and consumes 45.7 mW from a 1.5-V supply. The measured TIA demonstrates a transimpedance figure of merit of 200.7 Ω pJ [23].

Taiyi Huang et al. [2011] discussed a novel wideband CMOS Regulated Cascode (RGC) transimpedance amplifier, which can be used in the front-end of 10 Gb/s optical communication system, that is implemented using a 0.18 µm CMOS process. Resistive feedback, source follower and capacitive degeneration techniques are used to increase bandwidth. The simulation results show that the transimpedance gain is 40 dBΩ, the bandwidth is 8.69 GHz and the average noise current spectral density is 96.48 pA/√Hz. The output eye-diagram voltage amplitude is 2.05 mV when the input current magnitude is 50 µA [24]. Behnam Sedighi et al. [2012] propose a new circuit for the realization of transimpedance amplifiers (TIAs), targeted at reducing the input referred noise of the TIA or alternatively increasing the bandwidth, without increasing the power dissipation. A prototype chip is fabricated in 0.25-µm SiGe BiCMOS technology, has a gain of 71 dBΩ, a bandwidth of 20.5 GHz, and an average input-referred current noise density of 18 pA/√Hz. The circuit operates from a 2.5-V supply, and power dissipation is 57 mW [25].

Luis B. Oliveira et al. [2012] discussed a low noise transimpedance amplifier (TIA) that is used in radiation detectors to transform the current pulse produced by a photo-sensitive device into an output voltage pulse with a specified amplitude and shape, and review the traditional approach, feedback TIA, using an operational amplifier with feedback, and investigate two alternative circuits: the common-gate TIA, and the regulated cascode TIA and derive the transimpedance function (the poles of which determine the pulse shaping); we identify the transistor in each circuit that has the dominant noise source, and obtain closed-form equations for the rms output noise voltage. A circuit prototype of a regulated cascode TIA is designed in a 0.35-µm CMOS technology, to validate the theoretical results by simulation and by measurement [26]. Chia-Wei Soong et al. [2013] introduces a high-temperature fully monolithic high gain-bandwidth 6H-SiC transimpedance amplifier for capacitive sensor interfacing. This amplifier achieves a gain of 235 kΩ and a bandwidth of 0.61 MHz at room temperature. Variable capacitors demonstrate the functionality of differential capacitive sensing across a wide temperature range, up to 450 °C. At elevated temperatures, the amplifier exhibits increasing gain with decreasing bandwidth, as expected. At 450 °C, the gain and bandwidth are 774 kΩ and 0.17 MHz, respectively. This demonstrates the capacitive sensing capability of a SiC transimpedance amplifier, and represents a critical step toward the goal of integrating a sensing element with its interface circuit in a single monolithic device for operation at extreme temperatures [27].

III. CONVENTIONAL CMOS CURRENT CONVEYOR

A new topology to offset the large junction capacitance brought by photodiode. It is achieved by creating a zero differential impedance at the input node of a TIA. This input stage is based on a cross-coupled current conveyor structure [16]. The TIA relaxes the bandwidth limitation at the input node, and exhibits a stable performance over a wide range capacitive load. This cross-coupled structure also brings a huge improvement in noise performance as the single-ended input-referred noise current of the overall circuitry. The shunt-inductive peaking [14] and capacitive degeneration techniques [15] are also employed for further bandwidth enhancement.
A cross-coupled current conveyor based TIA is studied. The input stage provides very low input impedance, relaxing the bandwidth limitation at the input node. The noise analysis also shows that the proposed input stage achieves more effective isolation of the photodiode capacitance from the bandwidth determination as compared to CG and RGC input stages. The cross-coupled structure facilitates the construction of a differential TIA circuit as well.

V REFERENCES


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