VLSI: Techniques for efficient Standard Cell Placement

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Abstract- In the physical designing of the chip, placement is one of the most important steps in the design flow, this paper gives the basic overview of the placement algorithms being used with shrinking technology node for the automatic placement of cells which gives an optimized design in terms of chip area, speed and cost. Basically the emphasis will be on recent trends of Wire-length driven placement (higher technology node) which includes the different ways to estimate wire length and also the Timing driven placement technique (lower technology node) i.e. by meeting the setup and hold time requirements (STA) of the design and thus bringing out the advancement and challenges in placement research techniques being used. Thereby concluding an efficient way of arranging the logic cells on VLSI chip.

I. INTRODUCTION

In the era of shrinking technology node of VLSI design, placement is the critical part of physical synthesis flow which has significant impact on the length of the wire in the design as well as the timing requirements which are to be met. The total quantity wire-length which is required by the design affects the chip’s design cycle and is frequently used as measure of quality placement, thus the focus is to minimize the total wire-length (TWL). However, with higher integration level on the chip and increased complexity of the design the factor other than optimized use of total wire-length is “congestion control” which is to be emphasized at the placement level. After placement the congested area will require more diversion from original route. Hence for estimating the wire-length we would require Manhattan geometry i.e. only horizontal and vertical lines are used to connect any two points. There are various methods of connecting the two pins which are as follows: Steiner tree, Minimal Spanning tree, Source-to-sink connection and most efficient of them is Half-perimeter bounding box method. Whereas, timing drive placement (TDP) is designed specifically targeting wires on timing critical paths. The TDP can be basically classified into two classes: net based and path based approach. The net based approach takes into consideration the nets of the critical paths and assumes that by taking care of the nets of critical paths we can optimize the delay of the paths. The path based approach deals with either all or subset of the paths to get optimized results. The other main category of classifying placement algorithm is: constructive placement and iterative improvement. In constructive algorithm, placement is done from the scratch and it is deterministic in nature whereas in iterative it starts with some initial placement and repeatedly modify it which is probabilistic in nature. This gives the basic idea about the placement of standard cells and macros.

II. WIRE-LENGTH DRIVEN PLACEMENT

The actual wiring paths are not known during placement. For making a decision a placement algorithm needs to model a topology of interconnection of nets. 

Wire-Length Estimation

Early work on wire length estimation was based on Rent’s rule which is based on empirical model. To get more accurate estimate of the wire length we should take into consideration actual route of routing. Almost all automatic tools use “Manhattan geometry” for two terminal nets. If the begin and end co-ordinates are \((x_1,y_1)\) and \((x_2,y_2)\) then the length of the wire is given by:

\[
L = |x_2 - x_1| + |y_2 - y_1|
\]
For estimation of length multi-terminal nets following techniques are used:

(i) **Half-Perimeter bounding box Method**: An efficient and commonly used method for estimating wire length is given by half the perimeter of the smallest rectangle enclosing all the pins. In case of Manhattan wiring it is more efficient for two and three terminal nets. However, it generally underestimates the wire length for higher degree nets.

![Figure 1. Half-Perimeter Wire length = X+Y](image)

(ii) **Steiner tree Method**: The route to connect all the points in the shortest way is defined by Steiner method[4],[5]. A wire can branch from any point along its length. For an undirected distance graph $G = (V,E,d)$ and set $S$, $V$ is the set of vertices, $E$ is the set of edges in graph $G$, $d$ is the distance function and $S$ is the subset to vertices $V$, so steiner tree problem is used to find a tree of $G$ that spans $S$ with minimal total distance on all its edges. But it is computationally expensive.

![Figure 2. Steiner Tree](image)

(iii) **Minimal Spanning Tree**: The branching is allowed at the pin locations only, hence the pins are connected in the form of minimal spanning tree. Using various known algorithms Minimal spanning tree can be constructed given the co-ordinates and the netlist. It is commonly used and is easy to compute.

![Figure 3. Minimal Spanning Tree (MST)](image)

(iv) **Source-to-sink connection**: The output pin of the module is connected to all input by separate wires. They are simplest to implement but it will effect the interconnect length and wiring congestion.

### III. CONGESTION

As the complexity of the VLSI chips is growing as the number of cell per design is increasing and the electrical property of metal wires are scaling poorly, hence it becomes necessary to estimate the congestion well before the placement step in order to avoid routing congestion. The wire length estimation may need to know congestion map of the circuit as most wires are likely to stray away from its original route for a portion of chip which is more congested. Thus we can conclude that wire-length estimation and congestion prediction are dependent on each other.
Thus to break the dependency probabilistic distribution model can be used to estimate the pin location and hence the wire-length. At an early stage of design flow especially for deep sub-micron technology having extremely high densities would result in the congestion problem. Over-congestion will lead to deteriorate the overall performance of the circuit, thus congestion model will play a vital role in predicting and estimating the congestion in early stages.

Congestion Classification

Congestion classification based on the type of interconnects: (i) Internal Congestion: Congestion at bin boundary is due to crossing of local interconnects. Since there is no specific information about the interconnects at the floorplanning stage [6] hence internal congestion is estimated by the L-shaped routing net and Rent’s rule (1-bend) which is given by:

\[ T = AC^P \]

which correlates the number of signal inputs \( C \) (number of gates) and output terminal \( T \) by a power law relation where \( A \) is rent’s coefficient i.e. average number of pins per cell and \( P \) is the feature parameter of the circuit.

(ii) External Congestion: Congestion at bin boundary is due to global interconnect. The simplest way to estimate the external congestion is real routing, Z-shape routing (2-bend).

The Lou et al. (ISPD-2001) assumes that every path has the same probability of occurrence and the Sidewinder pattern routes allow at most three bends per two pin nets. While routing the nets the following points must be considered: (a) avoid overflow i.e. exceeding the grid capacity (b) minimize the wire-length i.e. the total routed distance (c) bend count in the design should be minimum so as to avoid the change in metal layer.

Congestion Estimation: To estimate the wire-length and congestion of a placed standard cell. We will have to calculate the wire density [10] i.e. the probability that the particular line-segment \((x,y) \subseteq BB(t)\) (bounding box for net \( t \)) in fig.7

![Fig7. Bounding box for net t](image)

The faster way of estimating congestion than global routing method is probabilistic method as described in [1],[2] so as to get accurate results, but this method is not suitable for estimating congestion with design having obstacles.
IV. TIMING DRIVEN PLACEMENT (TDP)
The timing driven placement (TDP) targets specified wires depending on the timing critical paths. The timing driven placement can be performed at both global and detail placement stages. The timing driven placement can be broadly classified into:

(i) **Net-based** approach which deals with individual nets with (a) Net weight approach based on timing analysis higher weights are assigned to critical nets so as to reduce the lengths of critical nets and to improve the overall timing by reducing the delay. This approach is known for its simplicity but on the other hand it is more complex to assign weights to these critical nets. The net-weight approach can be classified into:

- **Static Net Weight Approach**: which deals with assigning the weights to the nets once before the placement and weights and the weights do not change even after the timing-driven placement takes place. Based on the following factors the weights can be assigned slack, cycle time, and fanout (criticality factors) FOM, WNS (sensitivity factors). Sensitivity factors have look-ahead mechanism which can see the impact of the net weights assigned on timing.

- **Dynamic Net Weight Approach**: This approach considers change in the timing report during and after placement and thus after analyzing the present timing report it again assigns weight to the nets. The accuracy with which weights are assigned gives more optimized timing, hence the problem oscillation arises i.e. with each iteration the length of critical and non-critical nets changes and accordingly the weights assigned to them.

(b) Net constraint approach: Net length constraint (NLC) serve as the threshold value to meet the timing requirements of the design and limits the total wire-length. Net constraint approach has more accurate control over net weight approach in minimizing the wire-length. So as to get more accurate results NLC bounds have to be defined more precisely to get optimal solution space.

(ii) **Path based Approach**: The path based timing driven placement makes sure that all the paths which are in consideration, will meet the timing requirement met after the placement. It is more complex approach as it considers timing of path in placement which may be restricted. It can be further classified in:

(a) Linear Programming (LP) based formulation: It considers the two sets of variable i.e. physical and electrical. The physical parameter constitutes the co-ordinates of the cell and net length and electrical parameters deals with delay associated with gates, nets and also the arrival time propagation through critical paths and at the endpoint. The objective would to increase the WNS.

(b) Stimulated Annealing method is time consuming but more accurate heuristic which is used for solving any optimization problem of placement. Basic phenomenon on which SA works is it accepts all the moves which tend to reduce the cost. Also the moves with increased cost are accepted with a probability that decreases with increase in cost. The temperature decides this acceptance probability exp (ΔC/T) where ΔC is increase in cost. Higher the temperature more such moves will be accepted as the temperature is gradually decreased the probability of such moves to be accepted is decreased.

V. CONCLUSION
As the chip size is reducing but its density is increasing hence placement plays an important role in both its functionality and performance. With wire-length driven placement for a design having macros will try to place all the flops near to the macro in order to reduce the length of the wire but this would increase the congestion and hence the routing problem would increase. Thus the WDP are suitable for lower technology nodes i.e. chips with larger area. Out of several ways of estimating the wire-length the rectangular bounding box method is the easiest and more suitable for design containing at most three terminals but for higher terminal nets its accuracy decreases. For higher terminal nodes it is recommended to use Steiner tree method as it covers all the pins within minimum possible distance. The industrial library uses interpolated lookup table models to characterize the standard cell. Both capacitive load and slew rate that play as the major factors in timing model as described in Aaron P. Hurst et al. The table shows the result of timing driven placement of different paths described in Table1 of Aaron P. Hurst et al.
Table 1.
The size column indicates number of placed instances for the design. The REG MMC column shows the MMC achieved for a completely placed design using our placement flow with equal weights attached to the wires. The COM MMC column shows the MMC achieved after placement using combinational slack- based weighting function for nets.

VI. REFERENCES